REMARKS

Claims 14-22, 24-34, 36 and 37 were pending in the present application. Claims 1-13, 23 and 35 have been withdrawn and new claims 38-40 are added herein. Thus, claims 14-22, 24-34, and 36-40 are now pending. The applicants respectfully request reconsideration and allowance of the present application in view of the above amendments and the following remarks.

The applicants would appreciate receiving an acknowledgement of the claim for priority under section 119 and a notice that all certified copies of the priority documents have been received.

Claims 14-22 and 24-25 are objected to as allegedly including the following informalities: the term "the trench" in line 8 of claim 1 should be changed to "a trench structure" and the term "the trench" in claim 17 should be changed to "the trench structure."

Applicants note however, that there is no line 8 of claim 1, and further note that claim 1 has been withdrawn. Therefore, the applicants believe that the objection should have been directed to claim 14. Regardless, the applicants do not believe that an amendment to change the term "trench" to "a trench structure" is necessary. One of ordinary skill in the art would easily understand the meaning of the term "trench". If the Examiner insists that such an amendment is necessary, applicants respectfully request that reasons be provided as to why the term "trench" should be amended to "trench structure". The applicants however have amended the term "the trench" in lines 5 and 6 of claim 14 into "a trench" to provided proper antecedent basis.

Claims 14, 15, 20, 21, 25, 26, 27, 32, 33, and 37 stand rejected under 35 USC §102(e) as being allegedly anticipated by Ishio et al. (US 6,653,702). The rejection is respectfully traversed.

The present invention is characterized in that the diffusion structures 2, 3, 4 including the multiple diffusion regions 20, 30, 40 are formed and then, the trenches 6 are formed to isolate

semiconductor components 2a-2d, 3a-3d, 4a-4e, ***and to define the size thereof.*** Each diffusion structure is larger than the corresponding semiconductor component. Therefore, the sizes of the respective semiconductor components can be set at arbitrary sizes according to necessary current capacities by changing the number of the diffusion regions 20, 30, 40 included by each one of the trenches. Thus, the diffusion regions are used as units when forming the trench to define the size and thus the capacity of each semiconductor component. In contrast, in Ishio et al., the trenches 14 are formed first, and then, the plural circuit elements 4-6 are formed by diffusion processes. Applicants further note that in Ishio, et al., the alleged diffusion structure 11 is not a diffusion structure but rather is a laminated substrate. Thus, Ishio et al. fails to disclose all the claimed features having the above described characteristic of the claimed invention. Therefore, the rejection of claims 14 and 26 should be reconsidered and withdrawn.

Claims 15, 20, 21, 25, and 27, 32, 33, and 37 by virtue of depending from claims 14 and 26 are allowable for at least the reasons set forth herein above. It is respectfully requested that the rejection of claims 15, 20, 21, 25, and 27, 32, 33, and 37 be reconsidered and withdrawn.

Claims 14, 15, 18, 19, 22, 24, 30, 31, 34, and 36 stand rejected under 35 USC §102(b) as being allegedly anticipated by Koyama et al. (US 2001/0032990). The rejection is respectfully traversed.

Koyama et al. also fails to disclose the claimed trench as discussed above. In support of the rejection, Figs 1 and 3 of Koyama et al. are cited. Applicants first note that Fig. 1 is an electric circuit diagram, so it is not clear how a trench structure can possibly be shown. Also, since Fig. 3 of Koyama et al. designates only a device 200, and since reference is made to a Fig. 8 of U.S. Patent No. 6,104,076, not of record, and withdrawn from issue, there is no support for the allegation that a trench structure is shown in Fig. 3. The Examiner is required to specifically point out where in the reference the claimed feature is disclosed, Since no specific indication has

been made as to what feature of Koyama et al. is alleged to amount to the claimed trench, the applicants submit that the Examiner has not met their requirement. Further, a *prima facie* case of anticipation has not been established since, Koyama et al. fails to disclose a trench as claimed, e.g. to isolate the semiconductor component and to define the size thereof. Thus, the rejection of independent claim 14 should be reconsidered and withdrawn.

Claims 15, 18, 19, 22, and 24, by virtue of depending from claim 14 are allowable for at least the reasons set forth herein above. Claims 30, 31, 34, and 36 are allowable by virtue of depending from claim 26. Applicants note that claim 26 is not specifically noted in the present rejection over Koyama, thus claims 30, 31, 34, and 36 are allowable by virtue of depending from claim 26 for at least the reasons set forth herein above with regard, for example, to the rejection over Ishio, et al. It is respectfully requested that the rejection of claims 30, 31, 34, and 36 be reconsidered and withdrawn.

Claims 14, 17, 25, 26, 27, 29, 32, 33, and 37 stand rejected under 35 USC §102(b) as being allegedly anticipated by Yamazaki (US 5,306,940). The rejection is respectfully traversed.

Yamazaki also fails to disclose the claimed trench, including for example, that the trench defines the size of the semiconductor component. While Yamazaki, at best, describes that U-trench 112 serves as an isolation region of a semiconductor component, no description is present in Yamazaki of the trench defining a size of a semiconductor component, particularly in view of other claimed features such as the claimed diffusion structure.

Accordingly, for at least the reasons set forth hereinabove, a *prima facie* case of anticipation has not properly been established in that the applied reference fails to disclose all the claimed features as required. It is respectfully requested that the rejection of independent claims 14 and 26 be reconsidered and withdrawn.

Claims 17 and 25, and 27, 29, 32, and 33, by virtue of depending from independent claims 14 and 26, are allowable for at least the reasons set forth hereinabove. It is respectfully requested therefore that the rejection of claims 17 and 25, and 27, 29, 32, and 33 be reconsidered and withdrawn.

Claims 16 and 28 stand rejected under 35 USC §103(a) as being allegedly unpatentable over Ishio et al. and Koyama as independently applied. The rejection is respectfully traversed.

Applicants first note that claims 16 and 28, by virtue of depending from independent claims 14 and 26, are allowable for at least the reasons set forth hereinabove. Moreover, claims 16 and 28 are independently allowable for the following reasons.

Applicants further note that Examiner admits that both Ishio et al. and Koyama fail to teach the feature of claims 16 and 28. Contrary to the Examiner's assertion, the thickness of 5μm is not a matter of routine experimentation. According to applicants' specification on page 17, lines 4 to 9 thereof,, the thickness of 5μm of the P-type diffusion layer (semiconductor layer) 15 is specifically and deliberately selected, after careful consideration by applicants, so that the trenches can be easily filled in with BPSG, for example to facilitate manufacture. As admitted, Ishio et al. and Koyama et al. do not explicitly teach that a semiconductor layer on an insulating layer is equal to or less than five microns as claimed. Thus a *prima facie* case of obviousness has not been established in that the references fail to teach or suggest all the claimed features as admitted by the Examiner.

Accordingly, it is respectfully requested that the rejection of dependent claims 16 and 28 be reconsidered and withdrawn.

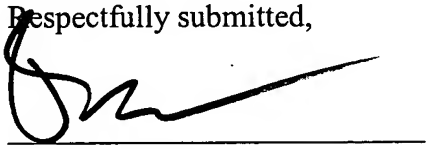
New claims 38-40 are submitted herein to more clearly distinguish over the applied art and contain features which should require no further search. For example, in claim 38 the feature of forming a diffusion structure *including a repeated pattern of diffusion regions*

common to the kind in an area of the substrate, in which the semiconductor component is to be formed is distinguishable over the prior art and was included in the originally claimed subject matter.

In view of the foregoing, the applicants respectfully submit that the present application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



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